Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**BASE**

**EMITTER**

**.019”**

**.019”**

**Top Material: Al**

**Backside Material: Au**

**E = .003 x .0032”**

**B = .003 x .0035”**

**Backside Potential: COLLECTOR**

**Mask Ref: 63**

**APPROVED BY: DK DIE SIZE .019” X .019” DATE: 10/4/21**

**MFG: FAIRCHILD THICKNESS .008” P/N: 2N3251**

**DG 10.1.2**

#### Rev B, 7/1